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METHOD OF FABRICATING A GATE DIELECTRIC LAYER FOR A THIN FILM TRANSISTOR

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The present invention relates to methods used to fabricate integrated circuits, and more specifically to a method used to form a gate dielectric layer for a thin film transistor.

(2) Description of Prior Art

Thin film transistors (TFT), have been used for specific integrated circuit applications. One such application for TFT devices have been in the area of liquid crystal display (LCD), panels. A transmissive - type LCD display panel comprises an array of light valves that selectively transmit incident light, in order to form an image on a display screen when the panel is backlit by a strong incandescent or fluorescent light source. Driving circuitry is provided to operate the light valves. Typically each light valve is energized by a TFT device, addressed along row and column addressing lines.

The TFT devices are comprised with a dielectric layer, used as the gate insulator layer, formed on a channel portion of an underlying active layer. For conventional metal oxide semiconductor field effect transistor (MOSFET), used for memory and logic applications, the gate

insulator layer is a thin silicon dioxide layer, thermally grown on an underlying single crystalline, silicon substrate. In contrast, the gate dielectric layer used in TFT applications, is grown, or formed on an underlying active region comprised of polysilicon. Unlike single crystalline silicon, this polysilicon layer is comprised of numerous small grains which create an uneven surface. The ability to thermally grow a gate dielectric layer, with the desired integrity in terms of leakage and breakdown, is adversely influenced by the unevenness of the underlying polysilicon surface, when compared to counterpart gate dielectric layers formed on underlying single crystalline silicon surfaces. Therefore a conventional gate dielectric layer formed on this uneven polysilicon surface will give inadequate TFT parametric integrity such as low gate breakdown voltage and high gate leakage current.

The present invention will describe fabrication procedures used to improve the integrity of a gate dielectric layer, for a TFT device, formed on an underlying active layer, such as polysilicon. The present invention will feature specific growth and anneal sequences for the TFT gate dielectric layer, which have demonstrated to improve the parametric performance of the overlying gate insulator layer. The present invention will also describe a novel process sequence, used to improve the integrity of a deposited gate dielectric layer. The deposited gate dielectric layer can either be used as an overlying component of a composite gate dielectric layer, comprised of the deposited layer on the underlying thermally grown gate dielectric layer, or used as the gate dielectric layer, directly on the underlying active layer. Prior art, such as Arghavani et al, in U.S. Pat. No. 6, 124,171, as well as Tai et al, in U.S. Pat. No. 6, 121,095, describe methods of forming silicon dioxide gate dielectric layers on underlying single crystalline silicon substrates,

however these prior arts do not describe the novel process sequence, introduced in this present invention, in which specific growth and anneal procedures are detailed for a composite gate dielectric layer, or for a thermally deposited gate dielectric layer, on an underlying, non-single crystalline, active layer.

SUMMARY OF THE INVENTION

It is an object of this invention to fabricate a thin film transistor (TFT), featuring a gate dielectric layer formed on an underlying polysilicon, active layer.

It is another object of this invention to form a gate dielectric layer on an underlying polysilicon, active layer, via thermal deposition of a silicon oxide layer, followed by an anneal cycle.

It is still another object of this invention to thermally grow a thin gate dielectric layer, on the underlying polysilicon active layer, followed by an anneal prior to thermal deposition of an overlying gate dielectric layer which has been shown to improve the TFT parametric performance.

In accordance with the present invention a method of forming a gate dielectric layer, for a TFT device, is described. An active layer of polysilicon is provided on an underlying insulator layer. For a first embodiment of this invention a thin, first dielectric layer is thermally formed, in an oxidizing ambient, on the underlying, polysilicon active layer. A first, in situ anneal cycle is then performed at a temperature greater than the temperature used for thermal growth of the thin

first gate dielectric layer. An overlying, second gate dielectric layer is next thermally deposited on the underlying thin, first gate dielectric layer, with the second gate dielectric thickness adjusted to meet circuit capacitance requirements. A second in situ anneal cycle is then performed to densify the second gate dielectric layer. Deposition of an overlying polysilicon layer is followed by patterning of the polysilicon layer, and of the composite gate dielectric layer, to form the gate structure for the TFT device. Formation of a source/drain region, in an area of the polysilicon active layer, not covered by the gate structure, complete the process sequence for the TFT device.

A second embodiment of this invention entails thermal deposition of the second gate dielectric layer directly on the top surface of the polysilicon active layer. An anneal procedure is then employed for densification purposes. Deposition of an overlying polysilicon layer, and patterning of the polysilicon layer and of the second gate dielectric layer, form the desired gate structure, followed by formation of the source/drain region.

BRIEF DESCRIPTION OF THE DRAWINGS

The object and other advantages of this invention are best described in the preferred embodiments with reference to the attached drawings that include:

Figs. 1 - 5, which schematically, in cross-sectional style, describe key stages of fabrication used to create a TFT device featuring a composite gate dielectric layer comprised of an underlying, thin thermally grown gate dielectric layer, and an overlying, thermally deposited gate dielectric layer.

Figs. 6 - 8, which schematically, in cross-sectional style, describe key stages of fabrication used to create a TFT device featuring a gate dielectric layer obtained via thermal deposition procedures.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The method of fabricating a gate dielectric layer, or composite gate dielectric layer, for a TFT device will now be described in detail. The TFT will be formed on an underlying insulating substrate 1. Any suitable insulating substrate may be employed, such as silicon oxide, sapphire, or preferably quartz. The first embodiment of this invention will describe a composite gate dielectric layer, comprised of an underlying, thin gate dielectric layer, thermally grown, and an overlying, thicker, gate dielectric layer, thermally deposited. The use of an underlying, thermally grown gate dielectric layer enhances the integrity of the composite gate dielectric layer, for example in terms of gate dielectric breakdown and TFT leakage characteristics, when compared to counterparts comprised with only one gate dielectric layer, thermally deposited directly on an underlying active layer. An active layer 10a, shown schematically in Fig. 1, is formed on insulating substrate 1. Active layer 10a, is a semiconductor material, such as a polysilicon layer, and is formed on insulating substrate 1, via a low pressure chemical vapor deposition (LPCVD), procedure between about 500 to 1500 Angstroms. A first, gate dielectric layer 22a, shown schematically in Fig. 1, is next thermally grown on active layer, or polysilicon layer 10a, at a temperature between about 800 to 1100° C, preferably about 900° C, in an oxidizing ambient,

such as a mixture of oxygen in argon or nitrogen. The thermal oxidation procedure performed for a time between about 15 to 30 min, results in the growth of a silicon dioxide, gate dielectric layer at a thickness between about 50 to 150 Angstroms, preferably 100 Angstroms. However the many small grains, and many grain boundaries contained in polysilicon layer 10a, cause surface roughness which results in a gate dielectric layer exhibiting lower integrity in terms of dielectric breakdown voltage and leakage, than counterpart gate dielectric layers that were thermally grown on single crystalline silicon substrates, comprised without small grains and numerous grain boundaries.

To improve TFT parametric performance, an anneal procedure is performed in an non-oxidizing ambient, resulting in active layer 10b. The anneal procedure is accomplished in situ, by increasing the temperature in the same furnace used for growth of first gate dielectric layer 22a, by an amount between about 10 to 20 %. This results in an anneal temperature between about 900 to 1200° C, preferably about 1000° C. This is schematically shown in Fig. 2. An inert ambient comprised of either nitrogen or argon is used for an anneal time of about 3 to 5 hrs. The time of anneal, between about 10 to 15 times longer than the oxidation time, again results in a TFT with improved device parametric performance when compared to counterpart dielectric layers, overlying an active layer comprised with smaller grains, thus more grain boundaries.

The second component of the composite dielectric layer, needed to satisfy the thickness requirement for the TFT gate dielectric layer, is next addressed and schematically described using

Figs. 3 - 4. A chemically vapor deposited, silicon oxide layer, is used for the thicker, second gate dielectric layer 24a. Second gate dielectric layer 24a, is obtained via thermal deposition procedures, using tetraethylorthosilicate (TEOS), as a source. Silicon oxide layers, obtained via TEOS thermally deposition procedures, have produced silicon oxide layers exhibiting greater uniformity when compared to silicon oxide layers obtained via plasma enhanced chemical vapor deposition (PECVD), TEOS procedures. Second gate dielectric layer 24a, is deposited to a thickness between about 500 to 700 Angstroms, to bring the total thickness of the composite dielectric layer to between about 550 to 850 Angstroms. Second gate dielectric layer 24a, shown schematically in Fig. 3, is thermally deposited at a temperature between about 600 to 700° C. To decrease porosity in the as deposited, second gate dielectric layer 24a, an anneal cycle is performed at a temperature between about 900 to 1000° C, in an ambient comprised of a mixture of argon or nitrogen, and oxygen. The annealing of second gate dielectric layer 24a, results in the creation of second gate dielectric layer 24b, comprised with less porosity, and improved device parametric performance, when compared to unannealed counterparts. The result of this procedure is schematically shown in Fig. 4.

The completion of the TFT device is next addressed and schematically shown in Fig. 5. A polysilicon layer 30, is deposited via low pressure chemical vapor deposition (LPCVD), procedures, to a thickness between about 3000 to 5000 Angstroms. Polysilicon layer 30, is either doped in situ, during deposition, via the addition of arsine or phosphine, to a silane ambient, or polysilicon layer 30, or externally doped in a diffusion tube by the use of PH_3 or $POCl_3$ gas sources, or polysilicon layer 30, is deposited intrinsically then doped via implantation of arsenic or

phosphorous ions. Conventional photolithographic and reactive ion etching (RIE), procedures, are then employed to pattern polysilicon layer 30, second gate dielectric layer 24b, and first gate dielectric layer 22b, creating gate structure 40. The RIE procedure used for definition of gate structure 40, employs Cl_2 or SF_6 as a selective etchant for polysilicon layer 30, while CHF_3 or CF_4 is used as an etchant for the gate dielectric layers, selectively terminating at the appearance of active layer 10b. After removal of the photoresist shape, used to define gate structure 40, source drain region 12, is formed in a region of active layer 10b, not covered by gate structure 40, via implantation of arsenic, or phosphorous ions, at an energy between about 50 to 100 KeV, and at a dose between about 1E15 to 1E16 atoms/cm^2. Subsequent processing steps used to produce a final TFT device, such as the addition of metal interconnect structures, and passivation layers, familiar to those skilled in the art, will not be described in detail here.

A second embodiment of this invention, featuring the use of a single, gate dielectric layer, is now described. Deposition of active layer, or polysilicon layer 10a, using identical conditions previously described in the first embodiment, is again used. A thermally deposited, gate dielectric layer 24a, obtained using TEOS as a source, is formed on active layer 10a, at a thickness between about 300 to 900 Angstroms, preferably 600 Angstroms, again using conditions identical to conditions previously used in the first embodiment, for deposition of second gate dielectric layer 24a. This is schematically shown in Fig. 6. To improve the density of the as deposited, gate dielectric layer 24a, an anneal procedure is performed, again using the identical anneal procedures applied to second gate dielectric layer 24a, in the first embodiment. The result of this anneal procedure is the creation of second, gate dielectric layer 24b, shown schematically in Fig. 7, on

active layer 10a. An anneal procedure, previously applied to active layer 10a, in the first embodiment, could be used if required in the second embodiment even though a thermally grown, first gate dielectric layer is not used. The conditions of this anneal are identical to those described in the first embodiment.

Gate structure 50, comprised of polysilicon layer 30, and second gate dielectric layer 24b, is next performed, using conventional photolithographic and RIE procedures, again using Cl_2 or SF_6 as an etchant for polysilicon, while using CHF_3 or CF_4 as an etchant for second gate dielectric layer 24b. Source/drain region 12, is again formed in regions of active layer 10a, not covered by gate structure 50. The result of these procedures are schematically shown in Fig. 8. The use of only a single, thick, gate dielectric layer, illustrated in the second embodiment, offers reduced process complexity when compared to the composite, gate dielectric layer, featured in the first embodiment. However the composite gate dielectric layer, featuring the use of the thermally grown, underlying dielectric component, provides improved device parametric performance, when compared to TFT devices comprised with only a single, thermally deposited, gate dielectric layer.

While this invention has been particularly shown and described with reference to, the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of this invention.